

# synchro/resolver to digital converter VMEbus 12, 14 or 16 bit series VME1686



# FEATURES

- Up to 6 channels
- 12, 14 or 16 bit resolution
- Accuracies to 1.3 arc minutes
- Tracking to 100rps
- ■50Hz to 10KHz excitation
- Continuous self-test
- Reference/signal loss alert
- Front panel status LED's
- 6U single card slot
- VME P1 bus slave
- VME backplane powered

# **GENERAL DATA**

The series VME1686 is a single-slot VMEbus card that incorporates up to 6 synchro or resolver to digital converters with resolutions of 12, 14 or 16 bits. The converters employ ratiometric conversion with a Type II servo loop necessary for high noise immunity and high speed performance. Sixteen bit converters feature a "reference synthesizer" required to maintain high accuracies even with large rotor to stator phase shifts or high rotational rates.

Each converter contains its own diagnostic circuitry. Diagnostics include loss of reference (LOR) and loss of stator signal (LOS) indicators. A built-in-test (BIT) feature is also incorporated that continuously monitors for excessive error. Three front panel summary status lamps give a visual indication of any of the above fault conditions. A memory location indicates the status of each reference and stator input plus the performance status of each converter.

# **ON-BOARD I/O DEVICES AND FUNCTIONS**

The VMEbus card contains the following devices and functions:

- Up to 6 synchro or resolver to digital converters
- Two Fault/Status registers
- Clear BIT Fault Control
- Test Register

## Synchro or Resolver to Digital Converters

Converters can be specified with 12, 14 or 16 bit resolutions and synchro or resolver input signals. The converters output a binary word representing the angular position of the synchro or resolver shaft. This word may be read out via the VMEbus at the offset specified in conjunction with the base address of the VME card. All converter channels continuously monitor for the presence of their respective reference and stator input voltages. Each converter also continuously monitors itself for excessive error or malfunction.

#### **Fault/Status Registers**

The Fault/Status Registers provide a means to obtain access to the fault and status outputs of all six converter channels via two read operations. These are word-wide (16 bit) read-only devices that are accessed via the VMEbus at the address offsets specified in conjunction with the base address of the VME card.

## **Clear BIT Fault Control**

This is a control function, not an I/O device. Due to the transient nature of the converter BIT outputs, the fault state of each BIT signal is latched on the card. During power-up, the BIT outputs are latched to a logic "1" state. This fault indication should be cleared via the VMEbus by reading or writing at the Clear BIT Fault address offset.

## **Test Register**

This is a byte addressable word-wide port built from two octal read-back latches. It may be accessed via the VMEbus by reading or writing to the Test Register address offset. The Test Register provides a dual purpose function. The primary role is as a diagnostic aid used to verify the functionality of the card's VMEbus interface circuitry and local data bus integrity. As a secondary role, the read-back latch capability on the card can be used at power-up to establish a level of confidence in the system's VMEbus.

## **SPECIFICATIONS**

Parameter		Value	
Resolution	12 bits	14 bits	16 bits
Accuracy <sup>(1)</sup>	±8.5 minutes	±4 minutes	±1.3 minutes
Tracking Rates	100rps max.	20rps max.	5rps max.
Power Supplies <sup>(2)</sup> +12V ±5% - 12V ±5% +5V ±5% Reference Input <sup>(3)</sup>	150mA 150mA 850mA	* * *	270mA 270mA *
Voltage	2.5-130Vrms	*	*
Frequency Impedance	47-10KHz	47-5.0KHz	47-2.6KHz
Single Ended	400KΩ	*	*
Differential	800ΚΩ	*	*
<b>Stator Inputs<sup>(3)</sup></b> Type	Solid state differential Synchro or resolver 2.5 to 115Vrms (L-L) 9V <sub>L-L</sub> KΩ		
Voltage Impedance			
Dynamic Characteristics	See S-R/Dcor	nverter specific	cation
TemperatureRangesOperating0° to +70°C (standard)-40° to +85°C (IT option)Storage-55° to +105°C			
NOTES: 1. Accuracy applies a) +10%, -20% s b) over specified c) 10% reference d) over specified e) over operating f) ±45° reference g) ±15° reference converters. 2. All DC power is p	tator amplitude reference voltage and stator harr power supply ra- temperature ra to stator phase to stator phase	ge and frequer nonic distortio anges. e shift, 16 bit c e shift, 12 and	n. onverters. 14 bit

- All DC power is provided via the VME P1 backplane connector. Power supply current values are absolute maximum.
- Reference and stator inputs are accessed via a front panel DC37P connector (J1). See Ordering Information for specific operating voltages and frequencies.
- 4. An \* indicates same as specification to the left.

# **I/O CONFIGURATION**

The VMEbus interface is configured as an A24:D16 slave. All data transfers to and from the card are via the VMEbus P1. The board monitors all Address Modifiers (AM5-AM0) and may be accessed via any of the following standard (A24) addressing modes:

Standard supervisory program access (3E) Standard supervisory data access (3D) Standard non-privileged program access (3A) Standard non-privileged data access (39)

The interface does not implement interrupt functions and will only transfer data if IACK\* is HIGH. The interrupt daisy chain is jumpered on board. After DSO\* or DS1\* goes LOW, DTACK\* will be driven LOW within 6 clock cycles of SYSCLK unless the converter is busy. Once the converter busy interval is complete, the DTACK\* will be driven LOW.

#### **Base Address Selection**

The VMEbus card base address is derived by partially decoding the VMEbus A24 address bus. Only the upper 8 lines (A23-A16) are monitored during VMEbus cycles. The card may be configured to respond to any one of 256 possible base addresses using the on board 8-position base address dip switch. This corresponds to the following VMEbus standard mode address range:

00xxxx hex to FFxxxx hex

Note: x = Don't care

Each of the 8 address select switches on the card corresponds to each of the 8 monitored address lines as follows:

VMEbus	CSI VMEbus Card
Address	Base Address Switch
A23	S1-8
A22	S1-7
A21	S1-6
A20	S1-5
A19	S1-4
A18	S1-3
A17	S1-2
A16	S1-1

The base address of the card may be set by placing each switch in the ON or OFF position to specify a particular address. The state of each switch corresponds as follows:

Switch State	Binary Value	Boolean State
ON	0	FALSE
OFF	1	TRUE

## **Offset Address Selection**

Each I/O device on the card may be addressed via a unique VMEbus address. The address for each I/O device is derived from the base address of the card and an offset value that is unique to each I/O device. The address offset value is combined with the card's base address to generate the VMEbus address used to access a particular I/O device on a particular card. The typical method used in the combination process begins by setting all "Don't care" bits in the base address to zero. Next, the desired offset value is simply added to the base address. This address is then used to access the I/O device via the VMEbus. The address offset value and access mode for each I/O device located on the CSI VMEbus card is summarized in the Address Offset Table.

ADDRESS OFFSET TABLE					
I/O Device Offset Data Port Access					
or Function	Hex	Width	Size	Туре	
S-R/D Chan 1	00	16 bit	word	read	
S-R/D Chan 2	02	16 bit	word	read	
S-R/D Chan 3	04	16 bit	word	read	
S-R/D Chan 4	06	16 bit	word	read	
S-R/D Chan 5	08	16 bit	word	read	
S-R/D Chan 6	0A	16 bit	word	read	
Clear BIT Fault	0C	n/a	word	read	
Clear BIT Fault	0C	n/a	word	write	
Fault/Status 1	0E	16 bit	word	read	
Fault/Status 2	10	16 bit	word	read	
Test Register	12	16 bit	word/	read	
Test Register	12	16 bit	byte	write	

# DATA LINES

The CSI VMEbus card provides 16 data lines configured as a D16 slave. The table below shows the format of the devices on the VMEbus card.

DATA LINE FORMAT TABLE				
Data S-R/D Fault Status			Fault Status	
Line	Data Bits	Register #1	Register #2	
D15	180.000°	not used	not used	
D14	90.000°	not used		
D13	45.000°	Chan 6 LOR	T I	
D12	22.500°	Chan 5 LOR		
D11	11.250°	Chan 4 LOR		
D10	5.625°	Chan 3 LOR		
D9	2.813°	Chan 2 LOR		
D8	1.406°	Chan 1 LOR		
D7	0.703°	not used	♥	
D6	0.352°	not used	not used	
D5	0.176°	Chan 6 LOS	Chan 6 BIT	
D4	0.088°	Chan 5 LOS	Chan 5 BIT	
D3	0.044°	Chan 4 LOS	Chan 4 BIT	
D2	0.022°	Chan 3 LOS	Chan 3 BIT	
D1	0.011°	Chan 2 LOS	Chan 2 BIT	
D0	0.006°	Chan 1 LOS	Chan 1 BIT	

**NOTE:** BIT = Built-in-Test

LOR = Loss of Reference Input LOS = Loss of Stator Input

BIT "0" = normal operation BIT "1" = excessive error LOR "0" = reference excitation ON LOR "1" = reference excitation OFF LOS "0" = stator input connected

LOS "1" = stator input disconnected

#### SYNCHRO/RESOLVER INPUT CONNECTOR (J1)

Pin #	ldent
$\begin{array}{c} 1\\ 2\\ 3\\ 4\\ 5\\ 6\\ 7\\ 8\\ 9\\ 10\\ 11\\ 12\\ 13\\ 14\\ 15\\ 16\\ 17\\ 18\\ 19\\ 20\\ 21\\ 22\\ 23\\ 24\\ 25\\ 26\\ 27\\ 28\\ 29\\ 30\\ 31\\ 32\\ 33\\ 34\\ 35\\ 36\\ 37\end{array}$	Chan 3 Ref Lo Chan 3 Stator S4 Chan 3 Stator S2 Chan 6 Stator S2 Chan 6 Stator S2 Chan 6 Ref Lo Chan 5 Ref Lo Chan 2 Ref Lo Chan 2 Stator S4 Chan 2 Stator S2 Chan 5 Stator S2 Chan 5 Stator S2 Chan 5 Stator S2 Chan 1 Stator S3 Chan 1 Ref Hi Chan 1 Ref Hi Chan 3 Stator S3 Chan 4 Stator S3 Chan 3 Stator S3 Chan 3 Stator S3 Chan 6 Stator S3 Chan 6 Stator S3 Chan 6 Stator S3 Chan 2 Ref Hi Chan 2 Ref Hi Chan 2 Ref Hi Chan 2 Ref Hi Chan 2 Stator S3 Chan 3 Stator S3 Chan 4 Stator S3 Chan 6 Stator S3 Chan 6 Stator S3 Chan 6 Stator S3 Chan 7 Stator S3 Chan 7 Stator S3 Chan 8 Stator S3 Chan 9 Stator S3 Chan 9 Stator S3 Chan 1 Stator S3 Chan 1 Stator S3 Chan 1 Stator S3 Chan 5 Stator S3 Chan 5 Stator S1 Chan 1 Ref Lo Chan 1 Ref Lo Chan 1 Stator S4 Chan 4 Stator S4 Chan 4 Stator S4

# ANALOG INPUTS

The synchro to digital converter signal designators S1-S2-S3 and RH-RL are described by the following equations:

$$\begin{split} & \mathsf{E}_{\mathsf{S1}\text{-}\mathsf{S3}} = \mathsf{KE}_{\mathsf{RL}\text{-}\mathsf{RH}}\mathsf{SIN}\Theta \\ & \mathsf{E}_{\mathsf{S3}\text{-}\mathsf{S1}} = \mathsf{KE}_{\mathsf{RL}\text{-}\mathsf{RH}}\mathsf{SIN}(\Theta + 120^\circ) \\ & \mathsf{E}_{\mathsf{S2}\text{-}\mathsf{S1}} = \mathsf{KE}_{\mathsf{RL}\text{-}\mathsf{RH}}\mathsf{SIN}(\Theta + 240^\circ) \end{split}$$

#### **ORDERING INFORMATION**

Resolver to digital converter signal designators S1-S2-S3-S4 and RH-RL are described by the following equations:

 $E_{S1-S3} = KE_{RL-RH}SIN\Theta$  $E_{S4-S2} = KE_{RL-RH}COS\Theta$ 

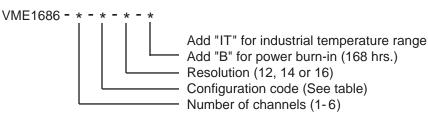
Where: K = synchro or resolver transformation ratio  $\Theta =$  synchro or resolver shaft angle in degrees

CONFIGURATION TABLE				
Code	Input Type			Stator Voltage
01 02 03 04	Synchro Synchro Synchro Resolver	26Vrms 115Vrms 115Vrms 26Vrms	360-2600Hz 360-2600Hz 47-2600Hz 360-2600Hz	11.8V 90.0V 90.0V 11.8V

## NOTES:

- 1. This is only a partial listing of configurations available.
- 2. Models may be supplied with a mix of converters, i.e., synchro and resolver, 12, 14 and 16 bit resolutions and multiple voltages and frequencies. Consult factory for special requirements.
- 3. The CSI VME1686 uses the 468A100, 468A300 and the 468H100 synchro or resolver to digital converters. Refer to those data sheets for additional specific information.
- 4. The part numbering designation system shown below may be used only when all converters on a card are identical.

#### PART NUMBER DESIGNATION



## WARRANTY

All units are warranted against defects in materials and workmanship for 1 year from the date of shipment. Liability is expressly limited to servicing, adjusting, or replacing any CSI product returned to our factory with delivery charges prepaid. In no case shall our liability exceed the original purchase price.